

Amendments to the Specification:

Please replace the paragraph beginning at page 1, line 4 with the following amended paragraph:

Until the advent of Coplanar Waveguides (CPWs), microstrip line was the conventional broadband transmission medium employed for use in electronics operating at the microwave and millimeter wave frequency bands. However, the major drawback with microstrip line is the difficulty encountered in placing series and shunt components on the same surface as the microstrip signal conductor. The problem arises because the ground conductor - to which electrical contact is essential for the operation of many components - is conventionally formed on the backside of a substrate (e.g. dDuroid, ceramic, etc.) on which the microstrip line is formed. Consequently, conductor-filled via holes through the substrate must be made to connect components on the topside of the substrate with the ground conductor (i.e. ground plane) on the bottom side of the substrate. The conducting material used in the via holes adds parasitics, such as unwanted inductances and resistances, to circuits assembled on the top side of the substrate. The parasitics in many cases lead to limits on the high frequency performance of the microstrip lines and circuits that include them.

Please replace the paragraph beginning at page 2, line 3 with the following amended paragraph:

Ideal CPW transmission lines would have expansive substrates and ground planes. However, such a structure is impractical to construct. Accordingly, conventional substrates used have a finite thickness (and width) and each of the ground conductors must also have a finite width. Beyond these two approximations, other refinements can be made in order to tailor the performance of the CPW structure so that CPWs may be integrated into various microwave or ~~millimeter wave~~ millimeter wave circuits and assemblies (e.g. packages).

Please replace the paragraph beginning at page 2, line 23 with the following amended paragraph:

CBCPWs support modes which can be ~~categorised~~categorized into one of three groups: 1) transmission modes guided by the CPW slots (gaps) - of which there is usually just one known as the fundamental mode, which is utilized for the transmission of signals on the CPW; 2) parallel-plate modes guided between the CPW plane and the backside conducting plane; and 3) possible parallel-plate modes guided in the space between a cover (above the CPW plane) and the signal conductor. The third group of modes (possible parallel plate modes) is relatively less important since the cover can usually be moved far enough away from the top for CPW to avoid the unwanted effects. Of the second group, only the lowest order mode is usually present but the second group serves as a detrimental vehicle for energy leakage from the fundamental mode supported by the CPW. Leakage occurs when the phase velocity of the parasitic mode(s) is slower than the phase velocity of the fundamental mode. Generally, the leakage is a continuous function of frequency with a leakage angle that varies such that the parasitic mode phase velocity projected along the fundamental mode direction matches the fundamental mode phase velocity. In a conductor-backed CPW, the backside conductive plane parallel-plate mode is generally slower than the fundamental CPW mode (in terms of phase velocity) and thus energy leakage occurs at all frequencies.

Please replace the paragraph beginning at page 3, line 18 with the following amended paragraph:

For example, in OC768 based systems, 40 Gbps opto-electronic networks require undistorted transmission of picosecond pulses over optical and electronic transmission media. Compared to the generation and characterization of picosecond electrical pulses, which is an almost fully matured technology, the development of transmission structures capable of handling the extremely wide bandwidth of these pulses still remains difficult. For electrical pulses a few

tens of picoseconds in duration, modal dispersion due to the physical dimensions (i.e. geometry) of the transmission media is the dominant factor contributing to ~~pulse distortion~~ pulse distortion.

Please replace the title on page 4 at line 9 with the following amended title:

SUMMARY OF THE INVENTION

Please replace the title on page 5 at line 15 with the following amended title:

DESCRIPTION OF THE DRAWINGS

Please replace the title on page 6 at line 7 with the following amended title:

DETAILED DESCRIPTION OF THE INVENTION

Please replace the paragraph beginning on page 7, line 8 with the following amended paragraph:

Figure 2 shows a CPW structure 200 that includes a substrate 30 and a signal conductor 20. The CPW structure 200 has ground conductors 24 and 25 that wrap around from a top surface 99 of the substrate 30 onto the lateral faces 98 of the substrate 30. Having the ground conductors 24 and 25 extend around and over the lateral faces of the substrate provides the CPW structure 200 with an electrical side-wall boundary that ~~is operation~~ acts to mitigate the effects of spurious mode generation. Suppression of spurious modes will be discussed in greater detail below.

Please replace the paragraph beginning on page 6, line 22 with the following amended paragraph:

In an implementation shown, ground conductors 24 and 25 electrically contact a metal package base 52 on planes parallel to the lateral faces 98 of the substrate 30. Implicitly the ground conductors 24 and 25 are biased to a same potential as the package base 52 since there is

a physical connection between each of the ground conductors 24 and 25 and the package base 52. The package base 52 is further adapted to support (suspend) the substrate 30 in a position above a cavity 70. In one implementation, the cavity 70 is filled with a material having a lower dielectric constant than the substrate 30. In one implementation, the cavity 70 is filled with air. Package base 52 provides ledges ~~53a, b~~ 53a, 53b (or in other embodiments ribs, spaced conductive pillars or a dielectric block that runs under the length of the substrate 30) on which the substrate 30 rests. In one implementation, the cavity 70 runs substantially the entire length of the substrate 30 in the transmission direction (into or out of the cross-section). The ledges ~~53a, b~~ 53a, 53b, and thus the substrate, are a height h above a substantially flat surface 56 also defined by the package base 52. Package base 52 can be milled from a solid piece of material or formed from casting material in the configuration shown in Figure 2.

Please replace the paragraph beginning on page 8, line 15 with the following amended paragraph:

Figures 3-6 described below illustrate the above four scenarios of CPWs packaged with MMICs of different heights (or thickness). The height of the MMIC for the above definition can also include the height of any electrical insulator needed to electrically isolate the backside of the MMIC from the package base 52. The height of the MMIC includes the height of any electrical insulator to account for cases where the MMIC backside metallization requires a DC voltage on the backside metallization in operation and thus needs to be isolated from the package base 52.

Please replace the paragraph beginning on page 9, line 15 with the following amended paragraph:

Fig. 3 shows an MMIC 305 packaged with a CPW on a common package base 52. As in the embodiment of Fig. 2, the CPW of Fig. 3 includes a signal conductor 20. In the scenario of Fig. 3, the MMIC 305 is thicker than the substrate 310. The cavity 70 is chosen so that the top of the substrate 310 is substantially flush with the top of the MMIC 305. As in the embodiment of Fig. 2, the substrate itself 310 has edge plating 25 in a wrap-around fashion that includes a

narrow strip of metallization on the bottom side 320 to the extent that the bottom side 320 rests on the metal package ledge 53. Thus the substrate 52 has sidewalls that confine and bound the electromagnetic energy within the substrate 52.

Please replace the paragraph beginning on page 10, line 1 with the following amended paragraph:

Fig. 4 shows a scenario of MMIC packaging where the MMIC 305 is substantially a same thickness as the CPW substrate 310. As in the embodiment of Fig. 2, the CPW of Fig. 3 includes a signal conductor 20 and a coplanar ground conductor 25. In the scenario of Fig. 4, the MMIC 305 is attached to a raised feature 315 in the package base 52, such as a pedestal or a Kovar tab. The raised feature 315 is chosen to be subsequently the same thickness as the depth of the cavity 70 underneath the substrate 310. The raised ~~feater~~feature 315 ensures that the top surface of the substrate 310 and the MMIC 305 are substantially flush, requiring only a short wire or ribbon bond to connect them resulting in low inductance. Low inductance for the bonds results in good return loss of interconnect between substrate 30 or 310 and MMIC 305 which is a key requirement for maximum power transfer across the interconnect over a broad range of frequencies.

Please replace the paragraph beginning on page 10, line 11 with the following amended paragraph:

Fig. 5 shows a scenario of MMIC packaging where the MMIC 305 is much thinner than the CPW substrate 310. As in the embodiment of Fig. 2, the CPW of Fig. 3 includes a signal conductor 20, a coplanar ground conductor 25, a package base 52 and a cavity 70. In the scenario of Fig. 5, the MMIC 305 is attached to a raised feature 315 (e.g. pedestal) of appropriate thickness so that the top surface of the substrate 310 and the MMIC 305 are once again substantially flush. As before, alignment of the substrate 310 with the MMIC 305 allows a short low inductance interconnect with wire or ribbon. Keeping the bond inductance low result in a high performance interconnect for high frequency broadband applications.

Please replace the paragraph beginning on page 10, line 18 with the following amended paragraph:

Fig. 6 shows a scenario of MMIC packaging where the thickness of the MMIC 305 is approximately equal to the ideal value of the depth of the cavity 70 plus the thickness of the CPW substrate 310. As in the embodiment of Fig. 2, the CPW of Fig. 3 includes a signal conductor 20 and a coplanar ground conductor 25. In such a case, the MMIC 305 may be attached to the flat surface of the package base 52. If not, the cavity depth is adjusted until the top surface of the MMIC 305 is substantially flush with that of the CPW substrate 310. The CPW substrate 310 may either be suspended on a cavity 70 and attached to a ledge, e.g., feature 53 in Fig. 3, with sidewalls that confine and align the CPW substrate 310. Alternatively, the CPW substrate 310 can be attached on raised ribs 600 running underneath the substrate forming a cavity 70 between a pair of ribs. The latter approach is chosen in situations when the MMIC 305 displays strong transverse resonances due to the proximity of the reflecting metal walls that form the sidewall of the substrate. Incorporating the cavity 70 for the CPW substrate 310 between raised ribs 600 instead of a ledge and cavity suspension approach eliminates the need for all metal walls at the MMIC and eliminates or mitigates most unwanted resonances.

Please replace the paragraph beginning on page 11, line 3 with the following amended paragraph:

Fig. 7 shows an MMIC 305 packaged with a CPW substrate 310 where the lateral face of the ground conductor 25 is electrically coupled to the base ~~56~~52 by a plurality of conductive ribs 700. As in the case of the embodiment of Fig. 2, the CPW also includes a signal conductor 20, an additional ground conductor 24, and a cavity 70. The configuration of Fig. 7 also exhibits the advantageous resonance suppression discussed above with respect to Fig. 6.

Please replace the paragraph beginning on page 11, line 7 with the following amended paragraph.

In addition to the variations illustrated above many of the distinguishing features of STCPW structures are possible in an asymmetric version of the CPW structure 200 that is otherwise implicitly symmetric. Referring again to Figure 2, ~~t~~The difference between an asymmetric CPW and symmetric CPW transmission line is that the respective spacings s_1 and s_2 between the signal conductor and each of the two ground conductors are equal for a so-called symmetric CPW structure and unequal on an asymmetric CPW structure.

Please replace the paragraph beginning on page 11, line 22 with the following amended paragraph:

A number of embodiments have been described. Nevertheless, it will be understood that various modifications may be made without departing from the spirit and scope of the invention. For example, Fig. 9 shows a multi-layer suspended CPW where the electrical side wall boundary function is performed by a plurality of conductive vias 900 connecting the co-planar ground conductors 24, 25 to a lower plane ground conductor (not shown). Such a structure is suitable for use in an environment where a ceramic substrate is employed for packaging multiple MMICs for a tighter level of integration.